**Abstract**

This circuit converts the PWM output signal from an RC receiver into an analog input signal on a 0V to 5V scale to the Sevcon Gen4 motor controller.

**Power Supply**

12V and GND enter the circuit through J1. The 12V rail is fed into U1, which provides a 5V rail at its output with . That rail is fed to U2, which uses high-frequency switching across C1 to generate a wavy -5V rail at its output with . C2 is placed across the output to smooth the -5V rail into a clean voltage.

**Signal Processing**

The PWM input signal enters the circuit through J2, which also powers the receiver from the 5V rail. Since the signal from the receiver is not designed to supply significant current, the voltage follower created by U3A replicates the signal. The output signal from U­3A is identical to the input signal, but U3A (as well as U3B, U3C, and U3D) can draw current from the dual power supplies connected to U3E and therefore does not suffer from the effects of loading as the receiver would. C3 and C4 serve as bypass capacitors for U3E.

When the signal exits U3A, it enters a low-pass filter composed of R1 and C5. The cutoff frequency of the filter is defined by , and the frequency of the PWM signal is Since fPWM is greater than fcutoff, the filter blocks the AC component of the input signal while passing its average voltage. The time constant of the filter is described by , so its response time is .

The logic level of the PWM signal is , and its positive pulse width varies between and . Its period is described by . Therefore, and . Thus, the average voltage of the PWM signal ranges between 250mV and 500mV.

Again, to avoid the effects of loading, the output voltage from the low-pass filter is repeated by a second voltage follower created by U3B.

The motor controller expects an analog input voltage on a 0V to 5V scale, and the circuit must be able to produce the entire voltage range. Thus, the input voltages must be linearly mapped to their corresponding output voltages. With a 250mV input voltage, the output voltage should be 0V. With a 500mV input voltage, the output should be 5V. Between the two extremes, the signal should scale linearly.

Basic algebra can be used to describe the relationship. Since the signal should scale linearly, is an appropriate equation. The slope can be calculated as . Then, the equation is rearranged to and the upper datapoint is substituted such that . The final equation becomes , where the gain is and the offset voltage is .

To produce these values, a zero-span circuit is created using U3C as an inverting summer. The values selected for R2, R3, R4, RV1, and RV2 are arbitrary, but the selected values define the gain of each component of the summer as . With the selected values for the pertinent circuit components, the summer approximately achieves one tenth times the inverse of the equation .

Finally, the signal enters U3D, which is configured as an inverting amplifier with a gain of . It inverts the signal from the inverting summer such that the desired equation is achieved. The output tracks the input linearly, with the input bounds tracking the output bounds as specified.

**Appendix A – Tuning**

Since error is present in the actual circuit due to noise, temperature, and small deviations from specified values of resistors and voltages, the circuit is designed with a provision for tuning. Since RV1 is series with R2, it is used to vary the value of the input resistor that defines the gain of the span. Likewise, RV2 can vary the input resistor for the offset of zero.

Note that when tuning the zero-span circuit, both tuning potentiometers affect the output for any given input signal. Therefore, only half of any error should be eliminated with RV1 or RV2 while tuning. The following procedure serves as an example.

1. Set the input PWM to its lowest duty cycle. The output should be 0V.
2. Remove half the error by manipulating RV1.
3. Set the input PWM to its highest duty cycle. The output should be 5V.
4. Remove half the error by manipulating RV2.
5. Repeat steps 1-4 as necessary until error is eliminated.

**Appendix B – Inverting Summer Calculations**

The calculations for the voltages and resistors used in the inverting summer circuit require an understanding of superposition. The inputs used for zero and span are both independent voltage sources, and they each have an effect on the output of the summer when the other source is disabled. For each input, the output voltage is dictated by the input voltage times the gain, as defined by . Therefore, the constant negative DC input voltage is multiplied by its gain to produce a positive DC output voltage, and the variable positive input voltage is multiplied by its gain to produce a variable negative output voltage. The summer combines the two signals to produce the inverse of the desired equation, and the final inverting amplifier inverts it once more.

To produce the zero and span values of the output equation, an inverting summer was used in conjunction with an inverting amplifier. A single noninverting summer could have been used to achieve the same effect, but the dual inversion in this circuit was chosen because it reduced the complexity of the gain calculations. However, it also prevented the inverting summer from producing the inverse of the desired equation at its full magnitude since the maximum required negative voltage of the equation is equal to the established negative rail voltage of -5V. and the op amps require a headroom voltage that prevents them from producing an output equal to their negative (or positive) rail. Instead, the inverting summer produces a tenth of its magnitude to remain between rail voltages, and the final inverting amplifier performs the final multiplication times 10.

The decision to use -5V as the constant DC input voltage to the inverting summer was somewhat arbitrary, driven by simplicity of the circuit used to invert the 5V rail and the availability of 5V regulators at the time of construction.

**Appendix C – Breadboarding**

If this circuit is not built on a protoboard or fabricated on a PCB, it can also be assembled on a breadboard. For simple wiring, the circuit should be constructed with the input on the left and the output on the right. The uppermost power bus should be set to +12V, the lowermost bus should be -5V, and the inner two busses should be set to GND. The 5V rail does not need a separate bus since it is fed only to the input of U2.

**Appendix D – Design**

This project was completed with the guidance and expertise of Professor J. M. Jacob, a Professor of Electrical Engineering Technology at Purdue University.